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High Performance Switches and Routers Broadband Packet Switching Technologies Quality of Service Control in High-Speed Networks Networking Systems Design and Development Next-generation IP Switches and Routers Interconnections for Computer Communications and Packet Networks Cloud Computing Networking Network Routing Packet Forwarding Technologies Computational Science - ICCS 2006 Computer Engineering and Technology Nonblocking Electronic and Photonic Switching Fabrics Interconnect-Centric Design for Advanced SOC and NOC Network Processors Advanced Detailed Router for Nanometer Designs with Hybrid Unilateral Monotonic (HUM) Routing Optical Interconnects for Future Data Center Networks Telecommunications and Networking — ICT 2004 TRANSMISSION, SWITCHING and ROUTING in communication networks Development of Routing Protocols for Mobile Ad Hoc Networks Bio-Inspired Fault-Tolerant Algorithms for Network-on-Chip Reconfigurable Networks-on-Chip Parallel and Distributed Processing and Applications Routing Algorithms in Networks-on-Chip Space Information Networks Selected Topics in Communication Networks and Distributed Systems Progress in VLSI Design and Test High-Speed Networking Advanced Routing of Electronic Modules High Performance Computing and Communications MMB & PGTS 2004 High Performance Design Automation for Multi-chip Modules and Packages Numerical Analysis and Its Applications Telecommunication Networks Multicore Systems On-Chip: Practical Software/Hardware Design AD HOC NETWORKS Management Enabling the Future Internet for Changing Business and New Computing Services Telecommunications Network Design and Management Asynchronous On-Chip Networks and Fault-Tolerant Techniques Networking and Telecommunications: Concepts, Methodologies, Tools, and Applications Parallel Computer Routing and Communication

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Network processors are the basic building blocks of today's high-speed, high-demand, quality-oriented communication networks. Designing and implementing network processors requires a new programming paradigm and an in-depth understanding of network processing requirements. This book leads the reader through the requirements and the underlying theory of networks, network processing, and network processors. It covers implementation of network processors and intergrates EZchip Microcode Development Environment so that you can gain hands-on experience in writing high-speed networking applications. By the end of the book, the reader will be able to write and test applications on a simulated network processor. Comprehensive, theoretical, and practical coverage of networks and high-speed networking applications Describes contemporary core, metro, and access networks and their processing algorithms Covers network processor architectures and programming models, enabling readers to assess the optimal network processor typer and configuration for their application Free download from http://www.cse.bgu.ac.il/npbook includes microcode development tools that provide hands-on experience with programming a network processor This is Volume IV of the four-volume set LNCS 3991-3994 constituting the refereed proceedings of the 6th International Conference on Computational Science, ICCS 2006. The 98 revised full papers and 29 revised poster papers of the main track presented together with 500 accepted workshop papers were carefully reviewed and selected for inclusion in the four volumes. The coverage spans the whole range of computational science. This book constitutes the refereed proceedings of the 16th International Symposium on VLSI Design and Test, VDAT 2012, held in Shibpur, India, in July 2012. The 30 revised regular papers presented together with 10 short papers and 13 poster sessions were carefully selected from 135 submissions. The papers are organized in topical sections on VLSI design, design and modeling of digital circuits and systems, testing and verification, design for testability, testing memories and regular logic arrays, embedded systems: hardware/software co-design and verification, emerging technology: nanoscale computing and nanotechnology. We are delighted to present the proceedings of the 12th Asia-Paci?c Network Operations and Management Symposium (APNOMS 2009), which was held in Jeju, Korea, during September 23–25, 2009. Recently, various convergences in wired and wireless networks, and conv- gence of telecommunications and broadcastings, are taking place for ubiquitous multimedia service provisioning. For example, broadband IP/MPLS wired n- works are actively converged with IEEE 802.11e wireless LAN, IEEE 802.16 Wireless MAN, 3G/4G wireless cellular networks, and direct multimedia bro- cast (DMB) networks. For e?cient support of service provisioning for ubiq- tous multimedia services on the broadband convergencenetworks, well-designed and implemented network operations and management functions with Q- guaranteed tra?c engineering are essential. The converged network will open the way for a new world with emerging new businesses and computing services. The Organizing Committee (OC) selected “Management Enabling the Future Internet for Changing Business and New Computing Services” as the timely theme of APNOMS 2009. Contributions from academia, industry and research institutions met these challengeswith173papersubmissions,fromwhich41high-qualitypapers(23.7% of the submissions) were selected for technical sessions as full papers, and 32 papers were selected as short papers. In addition, we had nine papers in - novation sessions for on-going research. Diverse topics were covered, including Tra?c Trace Engineering, Con?guration and Fault Management, Management of IP-Based Networks, Autonomous and Distributed Control, Sensor Network and P2P Management, Converged Networks and Tra?c Engineering, SLA and QoS Management, Active and Security Management, Wireless and Mobile N- work Management, and Security Management. Telecommunications Network Design And Management represents the state-of-the-art of applying operations research techniques and solutions across a broad spectrum of telecommunications problems and implementation issues. -The first three chapters of the book deal with the design of wireless networks, including UMTS and Ad-Hoc networks. -Chapters 4-6 deal with the optimal design of telecommunications networks. Techniques used for network design range from genetic algorithms to combinatorial optimization heuristics. -Chapters 7-10 analyze traffic flow in telecommunications networks, focusing on optimizing traffic load distribution and the scheduling of switches under multi-media streams and heavy traffic. -Chapters 11-14 deal with telecommunications network management, examining bandwidth provisioning, admission control, queue management, dynamic routing, and feedback regulation in order to ensure that the network performance is optimized. -Chapters 15-16 deal with the construction of topologies and allocation of bandwidth to ensure quality-of-service. "This multiple-volume publications exhibits the most up-to-date collection of research results and recent discoveries in the transfer of knowledge access across the globe"--Provided by publisher. System on chips designs have evolved from fairly simple unicore, single memory designs to complex heterogeneous multicore SoC architectures consisting of a large number of IP blocks on the same silicon. To meet high computational demands posed by latest consumer electronic devices, most current systems are based on such paradigm, which represents a real revolution in many aspects in computing. The attraction of multicore processing for power reduction is compelling. By splitting a set of tasks among multiple processor cores, the operating frequency necessary for each core can be reduced, allowing to reduce the voltage on each core. Because dynamic power is proportional to the frequency and to the square of the voltage, we get a big gain, even though we may have more cores running. As more and more cores are integrated into these designs to share the ever increasing processing load, the main challenges lie in efficient memory hierarchy, scalable system interconnect, new programming paradigms, and efficient integration methodology for connecting such heterogeneous cores into a single system capable of leveraging their individual flexibility. Current design methods tend toward mixed HW/SW co-designs targeting multicore systems on-chip for specific applications. To decide on the lowest cost mix of cores, designers must iteratively map the device’s functionality to a particular HW/SW partition and target architectures. In addition, to connect the heterogeneous cores, the architecture requires high performance complex communication architectures and efficient communication protocols, such as hierarchical bus, point-to-point connection, or Network-on-Chip. Software development also becomes far more complex due to the difficulties in breaking a single processing task into multiple parts that can be processed separately and then reassembled later. This reflects the fact that certain processor jobs cannot be easily parallelized to run concurrently on multiple processing cores and that load balancing between processing cores – especially heterogeneous cores – is very difficult. AD HOC NETWORKS: Technologies and Protocols is a concise in-depth treatment of various constituent components of ad hoc network protocols. It reviews issues related to medium access control, scalable routing, group communications, use of directional/smart antennas, network security, and power management among other topics. The authors examine various technologies that may aid ad hoc networking including the presence of an ability to tune transmission power levels or the deployment of sophisticated smart antennae. Contributors to this volume include experts that have been active in ad hoc network research and have published in the premier conferences and journals in this subject area. AD HOC NETWORKS: Protocols and Technologies will be immensely useful as a reference work to engineers and researchers as well as to advanced level students in the areas of wireless networks, and computer networks. As Internet traffic grows and demands for quality of service become stringent, researchers and engineers can turn to this go-to guide for tested and proven solutions. This text presents the latest developments in high performance switches and routers, coupled with step-by-step design guidance and more than 550 figures and examples to enable readers to grasp all the theories and algorithms used for design and implementation. Cloud computing is the most significant technology transformation since the introduction of the Internet in the early 1990s. As more and more companies and educational institutions plan to adopt a cloud-based IT infrastructure, today’s job market requires IT professionals who understand cloud computing and have hands-on experience developing cloud-based networks. Cloud Computing Networking: Theory, Practice, and Development covers the key networking and system administration concepts as well as the vital hands-on skills you need to master cloud technology. This book is designed to help you quickly get started in deploying cloud services for a real-world business. It provides detailed step-by-step instructions for creating a fully functioning cloud-based IT infrastructure using the Microsoft Azure cloud platform. In this environment, you can develop cloud services collaboratively or individually. The book enhances your hands-on skills through numerous lab activities. In these lab activities, you will learn to Implement the following services in a cloud environment: Active Directory, DHCP, DNS, and Certificate Services Configure Windows Server so it can route IP traffic Implement IP Security Policy and Windows Firewall with Advanced Security tools Create a point-to-site connection between Microsoft Azure and a local computer Create a site-to-site connection between Microsoft Azure and an on-premises network Develop a hybrid cloud that integrates Microsoft Azure with a private cloud created on a local network Cloud Computing Networking: Theory, Practice, and Development includes numerous examples, figures, and screen shots to help you understand the information. Each chapter concludes with a summary of the major topics and a set of review questions. With this book, you will soon have the critical knowledge and skills to develop and manage cloud-based networks. The explosion of traffic over data communications networks has resulted in a growing demand for Quality of Service (QoS) techniques to ensure network reliability, particularly in regard to e-commerce applications. Written by two experts in the field, this book covers the implementation of QoS techniques from an engineering point of view. Readers will find practical, up-to-date coverage of all key QoS technologies, real-world engineering examples illustrating theoretical results, and a discussion of new control techniques for the next generation multimedia networks. Market: Electrical Engineers and Computer Scientists involved with high-speed networks Effectively integrating theory and hands-on practice, Networking Systems Design and Development provides students and IT professionals with the knowledge and skills needed to design, implement, and manage fully functioning network systems using readily available Linux networking tools. Recognizing that most students are beginners in the field of ne Optical Interconnects in Future Data Center Networks covers optical networks and how they can be used to provide high bandwidth, energy efficient interconnects for future data centers with increased communication bandwidth requirements. This contributed volume presents an integrated view of the future requirements of the data centers and serves as a reference work for some of the most advanced solutions that have been proposed by major universities and companies. Collecting the most recent and innovative optical interconnects for data center networks that have been presented in the research community by universities and industries, this book is a valuable reference to researchers, students, professors and engineers interested in the domain of high performance interconnects and data center networks. Additionally, Optical Interconnects in Future Data Center Networks provides invaluable insights into the benefits and advantages of optical interconnects and how they can be a promising alternative for future data center networks. As Internet traffic continues to grow exponentially, there is a great need to build Internet protocol (IP) routers with high-speed and high-capacity packet networking capabilities. The first book to explore this subject, Packet Forwarding Technologies explains in depth packet forwarding concepts and implementation technologies. It covers the The telecommunications network is a global system of equipment and means that ensures the connections between the users of communication services, with the transmission and reception of the information involved. It is a set of communication nodes, in which processing procedures take place for the transmission and reception of information signals, switching connections and choosing routes between nodes to make connections

between sources and destinations of communications, and a set of links between these nodes, made in a variety of technologies. This volume contains 5 chapters in which the different processes and types of systems within the telecommunications network are presented. Network on Chip (NoC) addresses the communication requirement of different nodes on System on Chip. The bio-inspired algorithms improve the bandwidth utilization, maximize the throughput and reduce the end-to-end latency and inter-flit arrival time. This book exclusively presents in-depth information regarding bio-inspired algorithms solving real world problems focussing on fault-tolerant algorithms inspired by the biological brain and implemented on NoC. It further documents the bio-inspired algorithms in general and more specifically, in the design of NoC. It gives an exhaustive review and analysis of the NoC architectures developed during the last decade according to various parameters. Key Features: Covers bio-inspired solutions pertaining to Network-on-Chip (NoC) design solving real world examples Includes bio-inspired NoC fault-tolerant algorithms with detail coding examples Lists fault-tolerant algorithms with detailed examples Reviews basic concepts of NoC Discusses NoC architectures developed-to-date This book constitutes thoroughly revised selected papers of the 6th International Conference on Numerical Analysis and Its Applications, NAA 2016, held in Lozenetz, Bulgaria, in June 2016. The 90 revised papers presented were carefully reviewed and selected from 98 submissions. The conference offers a wide range of the following topics: Numerical Modeling; Numerical Stochastics; Numerical Approx-imation and Computational Geometry; Numerical Linear Algebra and Numer-ical Solution of Transcendental Equations; Numerical Methods for Differential Equations; High Performance Scientific Computing; and also special topics such as Novel methods in computational finance based on the FP7 Marie Curie Action,Project Multi-ITN STRIKE - Novel Methods in Compu-tational Finance, Grant Agreement Number 304617; Advanced numerical and applied studies of fractional differential equations. Surveys recent advances in combinatorial properties of switching fabrics Written by an expert in the area of switching fabrics Leading authorities deliver the commandments for designing high-speed networks There are no end of books touting the virtues of one or another high-speed networking technology, but until now, there were none offering networking professionals a framework for choosing and integrating the best ones for their organization's networking needs. Written by two world-renowned experts in the field of high-speed network design, this book outlines a total strategy for designing high-bandwidth, low-latency systems. Using real-world implementation examples to illustrate their points, the authors cover all aspects of network design, including network components, network architectures, topologies, protocols, application interactions, and more. Asynchronous On-Chip Networks and Fault-Tolerant Techniques is the first comprehensive study of fault-tolerance and fault-caused deadlock effects in asynchronous on-chip networks, aiming to overcome these drawbacks and ensure greater reliability of applications. As a promising alternative to the widely used synchronous on-chip networks for multicore processors, asynchronous on-chip networks can be vulnerable to faults even if they can deliver the same performance with much lower energy and area compared with their synchronous counterparts – faults can not only corrupt data transmission but also cause a unique type of deadlock. By adopting a new redundant code along with a dynamic fault detection and recovery scheme, the authors demonstrate that asynchronous on-chip networks can be efficiently hardened to tolerate both transient and permanent faults and overcome fault-caused deadlocks. This book will serve as an essential guide for researchers and students studying interconnection networks, fault-tolerant computing, asynchronous system design, circuit design and on-chip networking, as well as for professionals interested in designing fault-tolerant and high-throughput asynchronous circuits. This book provides a comprehensive survey of recent progress in the design and implementation of Networks-on-Chip. It addresses a wide spectrum of on-chip communication problems, ranging from physical, network, to application layers. Specific topics that are explored in detail include packet routing, resource arbitration, error control/correction, application mapping, and communication scheduling. Additionally, a novel bi-directional communication channel NoC (BiNoC) architecture is described, with detailed explanation. Written for practicing engineers in need of practical knowledge about the design and implementation of networks-on-chip; Includes tutorial-like details to introduce readers to a diverse range of NoC designs, as well as in-depth analysis for designers with NoC experience to explore advanced issues; Describes a variety of on-chip communication architectures, including a novel bi-directional communication channel NoC. From the Foreword: Overall this book shows important advances over the state of the art that will affect future system design as well as R&D in tools and methods for NoC design. It represents an important reference point for both designers and electronic design automation researchers and developers. --Giovanni De Micheli This volume contains revised versions of the 23 regular papers presented at the First International Workshop on Parallel Computer Routing and Communication (PCRCW '94), held in Seattle, Washington in May 1994. Routing for parallel computer communication has recently experienced almost explosive activity: ever increasing processor speeds are placing greater demands on interprocessor communication, while technological advances offer new capabilities to respond to those demands. The contributions from industry and academia cover all areas, from details of hardware design to proofs of theoretical results. There are also many papers dealing with the performance of various adaptive routing schemes, new network topologies, network interfaces, and fault-tolerant issues. Today's electronics industry requires new design automation methodologies that allow designers to incorporate high performance integrated circuits into smaller packaging. The aim of this book is to present current and future techniques and algorithms of high performance multichip modules (MCMs) and other packaging methodologies. Innovative technical papers in this book cover design optimization and physical partitioning; global routing/multi-layer assignment; timing-driven interconnection design (timing models, clock and power design); crosstalk, reflection, and simultaneous switching noise minimization; yield optimization; defect area minimization; low-power physical layout; and design methodologies. Two tutorial reviews review some of the most significant algorithms previously developed for the placement/partitioning, and signal integrity issues, respectively. The remaining articles review the trend of prime design automation algorithms to solve the above eight problems which arise in MCMs and other packages. This book constitutes the proceedings of the First International Conference on Space Information Network, SINC 2016, held in Kunming, China, in August 2016. The 18 full and 6 short papers presented in this volume were carefully reviewed and selected from 139 submissions. The theme of the conference encompasses new progress and development tendency of the space information network and related fields. There were 3 sections in the proceedings of SINC 2016 including the model of space information network and mechanism of high performance networking, theory and method of high speed transmission in space dynamic network, and sparse representation and fusion process in space information. The rapid growth of the electronic products market has created an increasing need for affordable, reliable, high-speed and high-density multi-layer printed circuit boards (PCBs). This book presents the technologies, algorithms, and methodologies for engineers and others developing the next generation of electronic products. A vision of the future in advanced electronics Advanced Routing of Electronic Modules provides both fundamental theory and advanced technologies for improving routing. Beginning chapters discuss approaches to approximate a minimum rectilinear Steiner tree from a minimum spanning tree and introduce ways to avoid obstacles for routing simple multi-terminal nets sequentially in a workspace. Timing delay, clock skew, and noise control requirements in signal integrity are described as well as computer-aided approaches to managing these requirements in high-speed PCB/MCM routing. Later chapters present the two-layer wiring problem, rip-up and reroute approaches, and parallel routing, including global routing, boundary crossing placement, and detailed maze routing in hardware acceleration. Data structures, data management, and algorithms for parallel routing in a multiple-processor hardware systems are also covered. Network Routing: Algorithms, Protocols, and Architectures, Second Edition, explores network routing and how it can be broadly categorized into Internet routing, PSTN routing, and telecommunication transport network routing. The book systematically considers these routing paradigms, as well as their interoperability, discussing how algorithms, protocols, analysis, and operational deployment impact these approaches and addressing both macro-state and micro-state in routing. Readers will learn about the evolution of network routing, the role of IP and E.164 addressing and traffic engineering in routing, the impact on router and switching architectures and their design, deployment of network routing protocols, and lessons learned from implementation and operational experience. Numerous real-world examples bring the material alive. Extensive coverage of routing in the Internet, from protocols (such as OSPF, BGP), to traffic engineering, to security issues A detailed coverage of various router and switch architectures, IP lookup and packet classification methods A comprehensive treatment of circuit-switched routing and optical network routing New topics such as software-defined networks, data center networks, multicast routing Bridges the gap between theory and practice in routing, including the fine points of implementation and operational experience Accessible to a wide audience due to its vendor-neutral approach This book constitutes the refereed proceedings of the 22nd CCF Conference on Computer Engineering and Technology, NCCET 2018, held in Yinchuan, China, in August 2018. The 17 full papers presented were carefully reviewed and selected from 120 submissions. They address topics such as processor architecture; application specific processors; computer application and software optimization; technology on the horizon. This book constitutes the refereed proceedings of the 5th International Symposium on Parallel and Distributed Processing and Applications, ISPA 2007, held in Niagara Falls, Canada, in August 2007. The 83 revised full papers presented together with three keynote are cover algorithms and applications, architectures and systems, datamining and databases, fault tolerance and security, middleware and cooperative computing, networks, as well as software and languages. This book provides a single-source reference to routing algorithms for Networks-on-Chip (NoCs), as well as in-depth discussions of advanced solutions applied to current and next generation, many core NoC-based Systems-on-Chip (SoCs). After a basic introduction to the NoC design paradigm and architectures, routing algorithms for NoC architectures are presented and discussed at all abstraction levels, from the algorithmic level to actual implementation. Coverage emphasizes the role played by the routing algorithm and is organized around key problems affecting current and next generation, many-core SoCs. A selection of routing algorithms is included, specifically designed to address key issues faced by designers in the ultra-deep sub-micron (UDSM) era, including performance improvement, power, energy, and thermal issues, fault tolerance and reliability. The effective design of high-speed, reliable switching systems is essential for moving the huge volumes of traffic and multimedia over modern communications networks. This book explains all the main packet-switching architectures, including all theoretical and practical topics relevant to the design and management of high-speed networks. Delivering the most systematic coverage available of the subject, the authors interweave fundamental concepts with real-world applications and include engineering case studies from wireless and fiber-optic communications. Market: Hardware and Software Engineers in the telecommunication industry, System Engineers, and Technicians. Many argue that telecommunications network infrastructure is the most impressive and important technology ever developed. Analyzing the telecom market's constantly evolving trends, research directions, infrastructure, and vital needs, Telecommunication Networks responds with revolutionized engineering strategies to optimize network construction. Omnipresent in society, telecom networks integrate a wide range of technologies. These include quantum field theory for the study of optical amplifiers, software architectures for network control, abstract algebra required to design error correction codes, and network, thermal, and mechanical modeling for equipment platform design. Illustrating how and why network developers make technical decisions, this book takes a practical engineering approach to systematically assess the network as a whole—from transmission to switching. Emphasizing a uniform bibliography and description of standards, it explores existing technical developments and the potential for projected alternative architectural paths, based on current market indicators. The author characterizes new device and equipment advances not just as quality improvements, but as specific responses to particular technical market necessities. Analyzing design problems to identify potential links and commonalities between different parts of the system, the book addresses interdependence of these elements and their individual influence on network evolution. It also considers power consumption and real estate, which sometimes outweigh engineering performance data in determining a product's success. To clarify the potential and limitations of each presented technology and system analysis, the book includes quantitative data inspired by real products and prototypes. Whenever possible, it applies mathematical modeling to present measured data, enabling the reader to apply demonstrated concepts in real-world situations. Covering everything from high-level architectural elements to more basic component physics, its focus is to solve a problem from different perspectives, and bridge descriptions of well-consolidated solutions with newer research trends. This book introduces different interconnection networks applied to different systems. Interconnection networks are used to communicate processing units in a multi-processor system, routers in communication networks, and servers in data centers. Queuing techniques are applied to interconnection networks to support a higher utilization of resources. There are different queuing strategies, and these determine not only the performance of the interconnection network, but also the set of requirements to make them work effectively and their cost. Routing algorithms are used to find routes to destinations and directions in what information travels. Additional properties, such as avoiding deadlocks and congestion, are sought. Effective routing algorithms need to be paired up with these networks. The book will introduce the most relevant interconnection networks, queuing strategies, and routing algorithm. It discusses their properties and how these leverage the performance of the whole interconnection system. In addition, the book covers additional topics for memory management and congestion avoidance, used to extract higher performance from the interconnection network. In Interconnect-centric Design for Advanced SoC and NoC, we have tried to create a comprehensive understanding about on-chip interconnect characteristics, design methodologies, layered views on different abstraction levels and finally about applying the interconnect-centric design in system-on-chip design. Traditionally, on-chip communication design has been done using rather ad-hoc and informal approaches that fail to meet some of the challenges posed by next-generation SOC designs, such as performance and throughput, power and energy, reliability, predictability, synchronization, and management of concurrency. To address these challenges, it is critical to take a global view of the communication problem, and decompose it along lines that make it more tractable. We believe that a layered approach similar to that defined by the communication networks community should also be used for on-chip communication design. The design issues are handled on physical and circuit layer, logic and architecture layer, and from system design methodology and tools point of view. Formal communication modeling and refinement is used to bridge the communication layers, and network-centric modeling of multiprocessor on-chip networks and socket-based design will serve the development of platforms for SoC and NoC integration. Interconnect-centric Design for Advanced SoC and NoC is concluded by two application examples: interconnect and memory organization in SoCs for advanced set-top boxes and TV, and a case study in NoC platform design for more generic applications. In this book, the focus is on the analysis and design of efficient, adaptive, and scalable routing protocols for Mobile Ad Hoc Networks. Next section presents the objective of the work performed in the context of this book. The main objective of this book is to develop routing protocols, which are appropriate for challenging environment of mobile ad-hoc networks. Given the inherent characteristics of these networks, the solutions must be adaptable to dynamic topologies, efficient with the bandwidth usage, scalable and energy efficient when various network parameters are concerned. Moreover, the focus is also on realistic approaches having relevance in real-life deployments. This means that the protocols should not be designed merely based on generic assumptions, which could lead to incorrect conclusions. Network Simulator (ns2.34) is the tools, which are used to determine that the developed algorithms are implementable in real networks. For validation in ad hoc networks, a specific scenario should also be mentioned for which the routing protocol has been designed. Meeting of these objectives includes providing the perception of the realities of ad-hoc networking. In addition, the proposed solutions should be compared against corresponding solutions found in the literature. New solutions must offer better performance with respect to others, to be able to contribute something to the research community. To summarize, the main goal of this book is to improve the knowledge in ad-hoc networking by providing solutions, which can help in developing new features for MANETs. This book will give the details of the methodology employed to achieve the goals. Welcometothe11thInternationalConferenceonTelecommunications(ICT2004)ho- ed by the city of Fortaleza (Brazil). As with other ICT events in the past, this professional meeting continues to be highly competitive and very well perceived by the international networking community, - tracting excellent contributions and active participation. This year, a total of 430 papers from 36 countries were submitted, from which 188 were accepted. Each paper was - viewed by several members of the ICT2004 Technical Program Committee. We were very pleased to receive a large percentage of top-quality contributions. Thetopicsofsubmittedpaperscoveredawidespectrumfromphotonictchniques,signal processing,cellularnetworks,andwirelessnetworks,toadhocnetworks.Webelievethatthe ICT2004papersofferawiderangeofsolutionstokeyproblemsintelecommunications, and describe challenging avenues for industrial research and development. In addition to the conference regular sessions, seven tutorials and a workshop were organized.Thetutorialsfocusedonspecialtopicsdealingwithnext-generationnetworks. The workshop focused on particular problems and solutions in heavily distributed and shareable environments. We would like to thank the ICT 2004 Technical Program Committee members and referees. Without their support, the creation of such a broad conference program would not be possible. We also thank all the authors who made a particular effort to contribute to ICT2004. We truly believe that due to all these efforts the ?nal conference program consisted of top-quality contributions. We are also indebted to many individuals and organizations that made this conference possible. In particular, we would like to thank the members of the ICT2004 Organizing Committee for their help in all aspects of the organization of this professional meeting.

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